What is claimed is:

1. An apparatus comprising:

groups of image sensors, each group comprising subgroup of sensors;

subgroup select circuits, each of which is coupled to an output from a respective subgroup of sensors;

group select circuits, each of which is coupled to outputs from subgroup select circuits associated with a respective one of the groups;

a bus coupled to outputs of the group select circuits; and

a controller for providing control signals to the subgroup select circuits and the group select circuits to selectively enable the respective subgroup select circuits and group select circuits to pass signals from the sensors to the bus one sensor at a time.

2. The apparatus of claim 1 wherein the sensors comprise active pixel sensors.

3. The apparatus of claim 1 comprising a charge sensing circuit electrically coupled to the bus.

4. The apparatus of claim 1 wherein the number of group select circuits is approximately equal to the square root of the number of subgroup select circuits.

5. The apparatus of claim 1 wherein a ratio of the number of subgroup select circuits to group select circuits is in a range of 10:1 and 40:1.

6. The apparatus of claim 5 wherein the ratio is in a range of 15:1 and 30:1.

7. The apparatus of claim 1 wherein each group select circuit comprises a transistor switch with a respective gate terminal for receiving a control signal from the controller, wherein when the switch is turned on, the group select circuit is enabled to pass signals from associated subgroup select circuits to the bus, and when the switch is turned off, the group select circuit is disabled from passing signals from the associated subgroup select circuits to the bus.

8. The apparatus of claim 7 wherein each subgroup select circuit comprises a transistor switch with a respective gate terminal for receiving a control signal from the controller, wherein when the subgroup select circuit switch is turned on, the subgroup select circuit is enabled to pass signals from an associated subgroup of sensors, and when the subgroup select circuit switch is turned off, the subgroup select circuit is disabled from passing signals from the associated subgroup of sensors to the bus.

9. The apparatus of claim 8 wherein the controller is configured for generating the control signals to enable and disable the group select circuit switches and the subgroup select circuit switches in a predetermined sequence.

10. The apparatus of claim 1 wherein the controller is configured to provide the control signals to enable the switches in the group select circuits sequentially, and, while a particular group select switch is enabled, to enable the subgroup select circuits associated with the particular group select circuit sequentially, one at a time.

11. The apparatus of claim 1 wherein the control circuit is configured to enable and subsequently disable each group select circuit, one at a time, in a sequential manner.

12. The apparatus of claim 1 wherein each group select circuit comprises a pair of NMOS transistor switches.

13. The apparatus of claim 1 comprising:

supergroups of sensors; and

supergroup select circuits, each of which is coupled to outputs from group select circuits associated with a respective one of the supergroups,

wherein the controller is configured to provide control signals to the supergroup select circuits to selectively enable a supergroup select circuit to pass a signal from the bus to another bus.

14. The apparatus of claim 13 wherein an output of each supergroup select circuit is coupled electrically to a common output bus.

15. The apparatus of claim 13 wherein each supergroup select circuit comprises a transistor switch with a respective gate terminal for receiving a control signal from the controller.

16. A method comprising:

(a) selectively enabling a group select circuit to electrically couple a charge mode read-out amplifier to a respective set of subgroup select circuits;

(b) when the group select circuit is enabled, enabling a pixel output signal to pass from each subgroup select circuit of the respective set of subgroup select circuits in a sequential manner through the group select circuit to the charge mode read-out amplifier; and

(c) disabling the group select circuit to electrically isolate the charge mode read-out amplifier from the respective set of subgroup select circuits.

17. The method of claim 16 further comprising repeating (a), (b) and (c) with respect to another group select circuit and respective set of subgroup select circuits.

18. The method of claim 16 wherein disabling the group select circuit occurs after a pixel output signal has passed from each subgroup select circuit in the respective set of subgroup select circuits through the group select circuit to the charge mode read-out amplifier.

19. A method comprising:

(a) selectively enabling a supergroup select circuit from a set of supergroup select circuits and a series-connected group select circuit from an associated set of group select circuits to electrically couple a charge mode read-out amplifier to a respective set of subgroup select circuits;

(b) when the series-connected group select circuit and supergroup select circuit are so enabled, enabling a pixel output signal to pass from each subgroup select circuit of the respective

set of subgroup select circuits in a sequential manner through the series-connected group select circuit and supergroup select circuit to the charge mode read-out amplifier; and

(c) disabling the group select circuit to electrically isolate the charge mode read-out amplifier from the respective set of subgroup select circuits.

20. The method of claim 19 further comprising repeating (a), (b) and (c) with respect to another series-connected group select circuit associated with the supergroup select circuit and a respective set of subgroup select circuits.

21. The method of claim 19 wherein disabling the group select circuit occurs after a pixel output signal has passed from each subgroup select circuit in the respective set of subgroup select circuits through the group select circuit and to the charge mode read-out amplifier.

22. The method of claim 19 further comprising disabling the supergroup select circuit to electrically isolate the charge mode read-out amplifier from the respective set of group select circuits and subgroup select circuits.

23. The method of claim 22 wherein disabling the supergroup select circuit occurs after a pixel output signal has passed from each subgroup select circuit in the respective sets of subgroup select circuits associated with each of the group select circuits through the supergroup select circuit and to the charge mode read-out amplifier.